

The Programmable Digital Frequency Program (PDFP)

This note reflects the knowledge gained about the functioning of the PDFP and its associated VME control module, the PDFP-CTRL. The information presented here was gathered by repeated attempts to interpret the original documentation, a lot of fiddling with the actual hardware, and by some educated guesswork. The task was complicated by the fact that only very little information about the internals of the electronics is accessible over the VMEBus.

The names of the various registers and the bits contained therein may not correspond with those of the original description. I've taken the liberty to re-assign names whenever I thought that would help comprehension.

The PDFP is a look-up table designed to hold a list of binary numbers representing the frequency of the accelerator cavities f_{RF} as a function of the magnetic field B . The PDFP keeps track of the magnetic field strength by counting the $B\uparrow$ and $B\downarrow$ pulses with a built-in counter. The corresponding table contents are presented on a 34-pin front panel connector. A second 34-pin connector accepts correction data which are added to the output. Six trigger inputs allow various actions, such as switching to a different table, clearing the B counter, or returning raw or corrected output values to take place at precise instants.

The PDFP-CTRL VME module

The PDFP is controlled by a VME module, the PDFP-CTRL, through a serial link running at 10Mbit/s. Data are exchanged 32 bits at a time and are buffered by a 256*32 FIFO. A number of accessory 16-bit registers controls some of the module's behaviour w.r.t. the VMEBus system. The module is accessible in the short IO address space. The base address is selected by setting jumpers connected to the address lines A15..A09. An installed jumper sets the corresponding address bit to '1'. The PS/CO preferred address in short IO space for this module is 0x2800.

Offset (in bytes) from base address	Register name	Description
0	fifo	32-bit data to be sent to PDFP
4	ctrl	Control and status register
6	base	Base address in STD IO range
8	ivec	Interrupt vector
0xa	ilvl	Interrupt level

Based on the register map above, a C-language structure describing the module could be defined as follows:

```
typedef struct {
    unsigned long fifo;
    unsigned ctrl,
        base,
        ivec,
        ilvl;
}pdfp;
```

The module also contains memory to store data received from the PDFP over the serial link. These data are stored in the form of 16-bit words at the address pointed to by a pointer register, which is incremented after each received word. The address at which this memory appears in the VMEBus standard address range is set by the contents of the *base* register in the short IO space.

Offset (in bytes) from base address	Name	Description
0	data	Data table
0x7ffe	ptr	Pointer register

A C-language structure matching this could be written as follows:

```
typedef struct {
    unsigned short data[0x3ffff];
    unsigned short ptr;
}pdfpmem;
```

Detailed register descriptions

Data written into the *fifo* register are sent to the PDFP module over a serial data link running at 10Mbit/s. A 256*32 FIFO buffers the data. This is a write-only register. Reading does not cause a bus error, but no valid data can be obtained.

The control and status register *ctrl*, controls and informs about the module's behaviour. The meaning of the bits are different for reading and writing. For writing, the allocations are as follows:

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ctrl	-	-	-	-	-	-	-	-	-	CDE	BCLR	PCLR	RxR	TxR	FHIE	FEIE

- FEIE Enables a VME interrupt when the FIFO is empty.
- FHIE Enables a VME interrupt when the FIFO crosses the half full boundary in either direction.
- TxR Resets the module's serial transmitter state machine.
- RxR Resets the module's serial receiver state machine.
- PCLR Clears the local pointer register.
- BCLR Clears the remote B-counter, in the PDFP NIM module, using the serial link. This doesn't seem to work.
- CDE Enable the counting direction of the local pointer register to be controlled by serial data coming back from the PDFP. If cleared, the pointer register can only be incremented. This feature is not tested (by us).

When read, the *ctrl* register bit allocations are these:

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ctrl	-	-	Stat	FF	FH	FE	TxEERR	RxEV	RxEP	MERR	BOF	TB4	TB3	TB2	TB1	TB0

Bits D07 to D00 come from the PDFP over the serial link, in response to an explicit status request. (See PDFP description below). There are a few microseconds of delay between the request and the updating of this field, due to the serial transmission. The remaining bits are local to the PDFP-CTRL module, and are not affected by delays.

- TB4..TB0 Look-up table currently in use on the PDFP. Only valid after status request.
- BOF PDFP B-counter overflow. Only valid after status request.
- MERR Memory error. Set when the memory bank currently selected doesn't exist. Note that this flag is unaffected by the value of the counter used to write into the PDFP tables. Only valid after status request.
- RxEP PDFP serial receiver error. Only valid after status request. Send command '1' to clear. (See below)
- RxEV PDFP-CTRL receiver error. Clear by writing RxR bit.
- TxEERR PDFP-CTRL transmitter error. Meaning unclear.
- FE PDFP-CTRL FIFO empty.
- FH PDFP-CTRL FIFO half (or more) full.
- FF PDFP-CTRL FIFO full.
- Stat Set when the PDFP has sent new status. Cleared after reading the *ctrl* register.

The *base* register contains the base address of the memory internal to the PDFP-CTRL module. Bits D04..D00 map to address bits A23..A19, and bit D07 enables access to the module's memory in

the VME standard address range. This register cannot be read back. The PS/CO preferred location in the standard address space for this module is 0x480000.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
base	-	-	-	-	-	-	-	-	E	-	-	A23	A22	A21	A20	A19

The *ivect* register contains the value of the interrupt vector applied to the bus during interrupt acknowledge cycles. The *ilvl* register holds the interrupt level that will be applied to the bus in case a condition arises which causes an interrupt. Neither register can be read back.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ivect	-	-	-	-	-	-	-	-	v7	v6	v5	v4	v3	v2	v1	v0
ilvl	-	-	-	-	-	-	-	-	-	-	-	-	-	12	11	10

In standard address space, the module essentially looks like an array of 0x3fff0 16-bit words. The eight even addresses from Std_base + 0x3fff0 to Std_base + 0x3fffe map to a single counter keeping track of data sent back to the PDFP-CTRL by the PDFP.

PDFP

The 4 most significant bits, C3..C0, of each 32-bit data word sent from the PDFP-CTRL to the PDFP are interpreted by the latter as a command code.

D31	D30	D29	D28	D27	//	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C3	C2	C1	C0		//	Parameter field																

The accepted command codes are as follows:

- 0 Status request. Upon reception of this code, the PDFP sends a status word back to the PDFP-CTRL over the serial link. The parameter field is ignored. After a suitable delay the information can be read from the *ctrl* register of the PDFP-CTRL module.
- 1 Clear serial link. This command clears the RxEP flag, which gets set in case the PDFP's receiver detects a communication error. The parameter field is ignored.
- 2 Set memory address pointer. Valid range depends on the size of the PDFP's memory. Setting out of range values here doesn't affect the MERR flag. Memory is contiguous. Look-up table boundaries are at 0x20000 word intervals
- 3 Fill memory. D26..D00 contain the data. The memory address pointer is automatically incremented after each word.
- 4 Not used.
- 5 Set PDFP mode. With D00 cleared, the 34-pin output connector presents the memory contents of the location pointed at by the B counter. With D00 set, it presents the sum of the memory contents and the data at the 34-pin input connector. Default value is D00 set.
The meaning of bit D01 is unclear.
- 6 Not used.
- 7 Not used.
- 8 Write trigger table. (See below).

Trigger table

The trigger table holds information about actions to be taken upon reception of a trigger signal on one of the six trigger inputs. Two extra entries in the table serve to either execute an action immediately, without waiting for a hardware signal, and to act upon the STB input. (?) The parameter field for a trigger table entry has the following format:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
-	T2	T1	T0	-	IB	OB	IS	OS	BCLR	TS	TB4	TB3	TB2	TB1	TB0

- T2..T0 Trigger table entry. A value of zero for this field results in the immediate execution of the action requested, or is associated with the strobe input, as appropriate. (See below). Values from 1 to 6 defer the action to the instant of reception of the associated trigger. (What if it's 7 ?)
- IB At each B \uparrow or B \downarrow pulse, send the value at the 34-pin input connector to the PDFP-CTRL through the serial link. This only works for trigger table entry 0.
- OB At each B \uparrow or B \downarrow pulse, send the value at the 34-pin output connector to the PDFP-CTRL through the serial link. This only works for trigger table entry 0.
- IS At each strobe pulse, send the value at the 34-pin input connector to the PDFP-CTRL through the serial link. This only works for trigger table entry 0.
- OS At each strobe pulse, send the value at the 34-pin output connector to the PDFP-CTRL through the serial link. This only works for trigger table entry 0.
- BCLR Clear the B-counter. The counter remains disabled until another trigger occurs with this bit cleared. The action is immediate if T2..T0 equals zero, or associated with the appropriate trigger if T2..T0 is 1..6.
- TS Select the look-up table according to the value of the TB4..TB0 field. The action is immediate if T2..T0 equals zero, or associated with the appropriate trigger if T2..T0 is 1..6.
- TB4..TB0 Look-up table to select.

The data sent back by the PDFP over the serial link to the PDFP-CTRL, in response to a strobe if IS or OS are set, or a B pulse if IB or OB are set, has the following format:

D31	D30	D29	D28	D27	//	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C3	C2	C1	C0	DIR	//	Data field																

- C3..C0 These bits hold a value which determines the interpretation of the remainder. Three interpretations are implemented.
- C3..C0 = 0: The data field holds status information, which is stored into the *ctrl* register.
 - C3..C0 = 6: The data field is a copy of the data present at the 34-pin input connector of the PDFP. It will be stored into the internal 128 kWord RAM at the address pointed at by the B-counter. The DIR bit tells the B-counter to which way to count..
 - C3..C0 = 7: The data field is a copy of the data presented on the 34-pin output connector of the PDFP. It will be written to the DPRAM port on the PDFP-CTRL front panel
- DIR This bit tells the B-counter whether the arriving word was the result of a B \uparrow or a B \downarrow pulse.
- D26..D0 This field holds the data, the interpretation of which depends on the C3..C0 field.

Examples:

- 0x10000000 Clear serial link.
- 0x00000000 Request status.
- 0x80000060 Select bank zero, clear and disable B-counter, immediately.
- 0x80001020 At trigger 1, select bank zero, enable B-counter.
- 0x80002021 At trigger 2, select bank one, B-counter enabled.
- 0x20020000 Set memory address pointer to the beginning of bank one.
- 0x37ffffff Write maximum value into first location of bank one. Address pointer now points at location 0x20001.

Notes & Questions

- Even though the fifo in the PDFP-CTRL has been defined as a long word, actual hardware access takes place as two consecutive short transactions with most VME processors currently in use. True long access is foreseen in the hardware, but is untested.
- Interrupt generation is untested.
- What happens if you set both IB and OB, or both IS and OS, in the trigger table?